JOYCEE MEKIE

ASSOCIATE PROFESSOR, ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY GANDHINAGAR
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Research Interests:

In-memory computing, Embedded memories, Approximate computing, Radiation hardened circuits/systems, Asynchronous circuits/designs, Asynchronous/Synchronous Network on chip architectures

Address: AB4/320, Department of Electrical Engineering,
IIT Gandhinagar, Near Palaj, Gandhinagar, 382355

Nationality : Indian
Gender: Female

EXPERIENCE

Associate Professor, Electrical Engineering, IIT Gandhinagar, Gujarat, 2021-ongoing
Assistant Professor, Electrical Engineering, IIT Gandhinagar, Gujarat, 2009 – 2021

Reader (Assistant Professor), Electrical Engg., M.S. University of Baroda, Gujarat, 2007-2009

Temporary Senior Research Assistant (during PhD), IIT Bombay, 2005-2007

Teaching Assistant (during PhD), IIT Bombay, Mumbai, 2001-2005

Lecturer, Electrical Engg., S. V. I. T Engg. College, Vasad, Gujarat, 2000-2001

Lecturer, Electrical Engg., S. V. M. I. T. Engg. College Bharuch, Gujarat, 1999-2000

Lecturer, Electrical Engg., V. V. P Engg. College, Rajkot, Gujarat, 1998-1999

Education

2009
PH.D. IN ELECTRICAL ENGINEERING, IIT BOMBAY
Thesis title: ***Interfacing solutions for Globally Asynchronous Locally Synchronous (GALS) systems***
GPA : 8.9 / 10

GRANTS

- "In Memory Computing for Next Generation Workloads Using Emerging Memory Technologies," Rs. 98,37,520/- SERB- SUPRA [Co-PI : Manu Awasthi, Ashoka University].
- "Fast, Robust, Energy-aware In-Memory Computing Architectures," $12000, Semiconductor Research Corporation, USA [Co-PI : Manu Awasthi, Ashoka University]
- "Comparative Study of Soft Error Tolerant Synchronous and Asynchronous Processors," Rs. 50,63,696, Science and Engineering Research Board (SERB), Department of Science and Technology (DST), 3 years, 29,23,000/-.
- "Estimating error probabilities due to multiple event transients in circuits designed for space applications based on electrical, temporal and logical masking," Rs. 6,60,000 MATRIC SERB-DST
- "Young Faculty Research Fellowship (YFRF), Rs. 37 Lakhs, Ministry of Electronics and Information Technology (MEITY), 2018-current, 2 years extendable to 5 years, Rs. 14,44,627.
- "Asynchronous and Synchronous approaches to Network-on-chip (NoC) architecture design," $12,000, Global initiatives on Academic network, 7-18 June, 2016.
- "Experimental studies of metastability in different synchronizers," Rs. 21,84,000, Department of Science and Technology (Fast-track scheme), 2012-2016.
- "Special manpower development project: Chips to System design (SMDP:C2SD)," Rs.70 lakhs plus VLSI Design and Device tools, Ministry of Electronics and Information Technology (MEITY), 2015-current, 5 years. [Co-PI]
- SMDP-C2SD - Chip Tape-out grant Rs. 9.83 Lakhs for testing "Radiation-hard-by-design Standard Cell Library" under SMDP-C2SD project, 2019-2020

GRANTS RECEIVED FOR STUDENT FELLOWSHIPS

- Intel PhD Fellowship [2014-2018] Sneha N. Ved
- Vivesvaraya PhD fellowship [2015-2019] and Intel PhD fellowship [2019-2020] for Chandan Kumar Jha
- Vivesvaraya PhD fellowship [2015-2020], Neelam Surana
- Prime Ministers Research Fellowship & Intel PhD Fellowship [2020-2021]. Kailash Prasad

THESIS SUPERVISED

DOCTORAL THESIS

1. Sneha N. Ved, "ASOCC: An Evaluation Framework for Asynchronous and Synchronous Network-on-Chip Architectures," Electrical Engineering
   Joined: July 2013 **Graduated: July 2020**
   (Intel PhD fellow)

2. Neelam Surana, "Opportunistic Context-Aware Energy-Efficient Embedded Memory Solutions," Electrical Engineering
   Joined: July 2015 **Graduated, August 2020**
   (Visvesvaraya PhD fellow)

3. Chandan Kumar Jha, "Approximate Designs and Frameworks for Error Resilient Applications," Electrical Engineering
   Joined: July 2015 **Graduated, November 2020**
   (Visvesvaraya PhD fellow)

4. Pramod Kumar Bharti, "Low energy Memories for approximate applications," Electrical Engineering
   Joined: July 2016 Ongoing (Expected to graduate by July 2023)

5. Tom Glint Isaac, "High Performance computing architectures," Electrical Engineering
   Joined: July 2017 Ongoing (Expected to graduate by December 2023)

6. Kailash Prasad, "Novel Hardware accelerators design and analysis," Electrical Engineering
   Joined: July 2018 Ongoing (Expected to graduate by July 2023)
   (Prime Minister's PhD fellow)

7. Arnav Banerjee, "In memory computing for ML acceleration," Electrical Engineering
   Joined: December 2022
   (Visvesvaraya PhD fellow)

MASTERS THESES

1. Jitesh Sah, "Framework for Synchronous to Asynchronous Design Conversion," July 2020.
2. Diptesh Datta, "Application-Centric Efficient SRAM/CAM/TCAM Memory Design." July 2020.
3. Ankita Nandi, "Co-optimizing Energy and Quality Using Approximate Designs and Techniques," July 2020.
4. Surendra Kumar, "Energy Efficient Sense-Amplifier Designs using Different Replica Circuits," July 2020.
5. Gyanendra Tiwari, "Design of Memory Compiler for Embedded Memories," July 2020.
6. Joydeep Kumar Devnath, "An approach towards building Energy Efficient Architectures for Neural Networks, 2019.

7. Arun Singh Tomar, “Configurable Approximate Circuits for Low Power FPGA based Applications,” 2019.
8. Mili Lavania, “Building Energy Efficient Radiation Hardened Memories and Memory Subsystem,” 2019.
9. Barma Abhishek, “High Performance Radiation Hardened Random Access and Content Addressable Memory Designs,” 2019.
10. Smriti Gupta, “Building of Radiation Hardened Processor Designs”, 2018.
11. Ishant, “Design of Radiation Hardened Memories and Memory Compiler”, 2018.
12. Shubhanshu Gupta, “Single and Double Node Upset Hardened Flip-Flops for Space Applications”, 2018.
13. Vishwanath Hiremath, “Approximate Neural Networks on FPGA”, 2018.
14. Neha Kumari, Impact of Process Variations & Technology Scaling on Synchronizer Performance,” 2017.
15. Hemal Shah, “Soft Error Tolerant Designs using Guarded Dual Rail Logic,” 2017.
16. Omkar Pujari, “Interfaces for Ratiochronous Network on Chips,” 2016.
17. Raminder Kaur, “Guarded Dual Rail Logic for Soft Error Tolerant Standard Cell Library,” 2016.
18. Fathima Sinin. “Study of Variability and Technology Scaling on Synchronizers and Design of Metastable-hard Synchronizers,” 2015.
19. Chandra Sekhar Tunga, “Design and implementation of efficient neuromorphic architectures”, 2015.
20. Bala Saranya Y, “Evaluating the scaling effects on synchronizers and global interconnects in multi-core SoCs,” 2014.

PUBLICATIONS

JOURNAL PUBLICATIONS

1. Sarabjeet Singh, Neelam Surana, Kailash Prasad, Pranjali Jain, Joycee Mekie, Manu Awasthi, “HyGain: High Performance, Energy-Efficient Hybrid Gain Cell based Cache Hierarchy,” *ACM Transactions on Architecture and Code Optimization*, 2022.

2. Datta, Diptesh, Neelam Surana, Anoop Kumar, and Joycee Mekie, “A 10T, 0.22fJ/Bit/Search Mixed-vt Pseudo Precharge-Free Content Addressable Memory.” *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2021. https://doi.org/10.1109/tcsii.2021.3103880

3. S. Walia, B. V. Tej, A. Kabra, J. Devnath and J. Mekie, "Fast and Low-Power Quantized Fixed Posit High-Accuracy DNN Implementation," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 1, pp. 108-111, Jan. 2022. doi: 10.1109/TVLSI.2021.3131609

4. C. K. Jha, S. Singh, R. Thakker, M. Awasthi and J. Mekie, "Zero Aware Configurable Data Encoding by Skipping Transfer for Error Resilient Applications," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 8, pp. 3337-3350, Aug. 2021.

doi: 10.1109/TCSI.2021.3081623

5. V. Gohil, S. Walia, J. Mekie and M. Awasthi, "Fixed-Posit: A Floating-Point Representation for Error-Resilient Applications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 10, pp. 3341-3345, Oct. 2021. doi: 10.1109/TCSII.2021.3072217

6. C. K. Jha, I. Doshi and J. Mekie, "Analysis of Worst-Case Data Dependent Temporal Approximation in Floating Point Units," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 2, pp. 767-771, Feb. 2021. doi: 10.1109/TCSII.2020.3012194

7. S. A. Aketi, S. Gupta, H. Cheng, J. Mekie and P. A. Beerel, "SERAD: Soft Error Resilient Asynchronous Design Using a Bundled Data Protocol," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 5, pp. 1667-1677, May 2020. doi: 10.1109/TCSI.2020.2965073

8. C. K. Jha, S. N. Ved, I. Anand and J. Mekie, "Energy and Error Analysis Framework for Approximate Computing in Mobile Applications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 2, pp. 385-389, Feb. 2020. doi: 10.1109/TCSII.2019.2910137

9. Bharti, Pramod K, N. Surana and J. Mekie, "Hetro8T: power and area efficient approximate heterogeneous 8T SRAM for H.264 video decoder," in *IET Computers & Digital Techniques*, vol. 13, no.6, pp. 505-513, 2019

10. N. Surana and J. Mekie, *"*Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications*," in IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 1023-1027, June 2019. doi: 10.1109/TCSII.2018.2869945

11. Ved Sneha N, Sarabjeet Singh and Joycee Mekie, "PANE: Pluggable Asynchronous Network-on-Chip Simulator," *ACM Journal Emerging Technologies in Computing Systems*, vol. 15, issue 1, article no. 7, January 2019, 27 pages. DOI: https://doi.org/10.1145/3241051

CONFERENCE PUBLICATIONS

1. K. Prasad, A. Biswas an J. Mekie, "PIC-RAM: Process-Invariant Capacitive Multiplier Based Analog In Memory Computing in 6T SRAM," *Design, Automation and Test in Europe (DATE),* 2023. [accepted]
   *Nominated for Best paper award.

2. T. Glint, M. Awasthi, J. Mekie, “REDRAW: Fast and Efficient Hardware Accelerator with REDuced Reads And Writes for 3D UNet,” *Design, Automation and Test in Europe (DATE)*, 2023. [accepted]
3. K. Prasad,A.Srivastava, N.Baruah, and J.Mekie “Fast and Robust Sense Amplifier Design for Digital IMC” (VLSID 2023)
4. K. Prasad*, T.Glint*, J.Dagli, K.Gandhi, A.Gupta, V.Patel, N.Shah and J. Mekie, “Hardware-Software Codesign of DNN Accelerators using Approximate Posit Multipliers,” *IEEE Asia and South Pacific Design Automation Conference (ASPDAC)*, 2023.
   *Nominated for Best paper award.

5. K.Prasad, J.Dagli, N.Shah, M.Pidagannavar, and J.Mekie “Impact of approximation and commutativity on Neural Network and Image Processing Applications.” *VLSI Design and Test (VDAT)*, 2022
6. Pramod Kumar Bharti, and Joycee Mekie. “RTQCC-14T: Radiation Tolerant Quadruple Cross Coupled Robust SRAM Design for Radiation Prone Environments”, *VLSI Design and Test (VDAT)*, 2022

7. K. Prasad*, A.Parmar*, N.Rao, and J. Mekie, “An Automated Approach to Compare Bit Serial and Bit Parallel In-Memory Computing for DNNs” *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022.
8. A.Parmar, K. Prasad, N.Rao, and J. Mekie, “FastMem: A Fast Architecture-aware Memory Layout Design” *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2022.
9. Pramod Kumar Bharti, and Joycee Mekie. "RHSCC-16T: Radiation Hardened Sextuple Cross Coupled Robust SRAM Design for Radiation Prone Environments", *IEEE International Conference on Computer Design (ICCD)*, 2022.
10. Pramod Kumar Bharti, and Joycee Mekie. “GBRHQ-14T: Gate Boosted Radiation Hardened Quadruple SRAM Design for Space Applications”, *IEEE International Conference on Emerging Electronics (ICEE)*, 2022.
11. K. Prasad, A. Biswas and J. Mekie, "Analysis of Word Line Shaping Techniques for In-Memory Computing in SRAMs," *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Dubai, United Arab Emirates, 2021, pp. 1-6. doi: 10.1109/ICECS53924.2021.9665469
12. C. K. Jha, S. Walia, G. Kanojia and J. Mekie, "FPCAM: Floating Point Configurable Approximate Multiplier for Error Resilient Applications," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021, pp. 1-5.
13. T. Glint, J. Sah, M. Awasthi and J. Mekie, "ANSim: A Fast and Versatile Asynchronous Network-On-Chip Simulator," *2020 IEEE 38th International Conference on Computer Design (ICCD)*, Hartford, CT, USA, 2020, pp. 619-622. doi: 10.1109/ICCD50377.2020.00107
14. J. K. Devnath, N. Surana and J. Mekie, "A Low-Voltage Split Memory Architecture for Binary Neural Networks," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, 2020, pp. 1-5. doi: 10.1109/ISCAS45731.2020.9180862
15. C. K. Jha, K. Prasad, A. S. Tomar and J. Mekie, "SEDAAF: FPGA Based Single Exact Dual Approximate Adders for Approximate Processors," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, 2020, pp. 1-5. doi: 10.1109/ISCAS45731.2020.9181185
    C. K. Jha, K. Prasad, V. K. Srivastava and J. Mekie, "FPAD: A Multistage

Approximation Methodology for Designing Floating Point Approximate Dividers," *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, 2020, pp. 1-5.

16. A. Nandi, C. K. Jha and J. Mekie, "Tunable Inexact Subtracters for Division in Image Processing Applications," *2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, 2020, pp. 1100-1103. doi: 10.1109/MWSCAS48704.2020.9184460
17. N. Surana, M. Lavania, A. Barma and J. Mekie, "Robust and High-Performance 12-T Interlocked SRAM for In-Memory Computing," *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Grenoble, France, 2020, pp. 1323-1326. doi: 10.23919/DATE48585.2020.9116361
18. J. K. Devnath, N. Surana and J. Mekie, "A Mathematical Approach Towards Quantization of Floating Point Weights in Low Power Neural Networks," *2020 33rd International Conference on VLSI Design and 2020 19th International Conference on Embedded Systems (VLSID)*, Bangalore, India, 2020, pp. 177-182. doi: 10.1109/VLSID49098.2020.00048
19. C. K. Jha, A. Nandi and J. Mekie, "Quality Tunable Approximate Adder for Low Energy Image Processing Applications," *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Genoa, Italy, 2019, pp. 642-645. doi: 10.1109/ICECS46596.2019.8965205
20. A. Nandi, C. K. Jha and J. Mekie, "Should We Code Differently When Using Approximate Circuits?," *2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Bangkok, Thailand, 2019, pp. 37-40. doi: 10.1109/APCCAS47518.2019.8953113
21. C. Jha and J. Mekie, "Design of Novel CMOS Based Inexact Subtractors and Dividers for Approximate Computing: An In-Depth Comparison with PTL Based Designs," *2019 22nd Euromicro Conference on Digital System Design (DSD)*, Kallithea, Greece, 2019, pp. 174-181. doi: 10.1109/DSD.2019.00034
22. C. K. Jha and J. Mekie, "SEDA - Single Exact Dual Approximate Adders for Approximate Processors ∗," *2019 56th ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, USA, 2019, pp. 1-2.
23. M. Lavania, N. Surana, I. Anand and J. Mekie, "Read-Decoupled Radiation Hardened RD-DICE SRAM Cell for Low-Power Space Applications," *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Xi'an, China, 2019, pp. 1-3. doi: 10.1109/EDSSC.2019.8753939
24. D. Datta, P. Dewangan, N. Surana and J. Mekie, "Energy and Area Efficient 11-T Ternary Content Addressable Memory for High-Speed Search," *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Xi'an, China, 2019, pp. 1-3. doi: 10.1109/EDSSC.2019.8754423
25. S. Gupta and J. Mekie, "Soft Error Resilient and Energy Efficient Dual Modular TSPC Flip-Flop," *2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID)*, Delhi, India, 2019, pp. 341-346. doi: 10.1109/VLSID.2019.00077
26. P. K. Bharti, N. Surana and J. Mekie, "Power and Area Efficient Approximate Heterogeneous 8T SRAM for Multimedia Applications," *2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded*

Systems (VLSID), Delhi, India, 2019, pp. 139-144.
doi: 10.1109/VLSID.2019.00043

27. J. Mekie, P. Mukim and K. Kale, "Impact of Variations on Synchronizer Performance: An Experimental Study," *2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID)*, Pune, India, 2018, pp. 459-460.
doi: 10.1109/VLSID.2018.112

28. S. A. Aketi, J. Mekie and H. Shah, "Single-Error Hardened and Multiple-Error Tolerant Guarded Dual Modular Redundancy Technique," *2018 31st International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems (VLSID)*, Pune, India, 2018, pp. 250-255.
doi: 10.1109/VLSID.2018.71

29. N. Kumari and J. Mekie, "Upset hardened latch as data synchronizer," *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hsinchu, Taiwan, 2017, pp. 1-2.
doi: 10.1109/EDSSC.2017.8126562

30. N. Surana, J. Mekie and N. R. Mohapatra, "Impact of high-κ spacer on circuit level performance of junctionless FinFET," *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hsinchu, Taiwan, 2017, pp. 1-2.
doi: 10.1109/EDSSC.2017.8126574

31. S. N. Ved, A. Bhange, A. Arya and J. Mekie, "Route-on-Fly: A single cycle router," *2017 4th International Conference on Signal Processing and Integrated Networks (SPIN)*, Noida, India, 2017, pp. 109-114.
doi: 10.1109/SPIN.2017.8049926

32. S. N. Ved, A. Arya, A. Bhange and J. Mekie, "A comparative study of input port and crossbar configurations in NoC router microarchitectures," *2017 4th International Conference on Signal Processing and Integrated Networks (SPIN)*, Noida, India, 2017, pp. 121-125.
doi: 10.1109/SPIN.2017.8049928

33. N. Surana, R. Kaur and J. Mekie, "Short and deep drain MOSFET for space applications: Device and circuit level analysis," *2016 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Bremen, Germany, 2016, pp. 1-4.
doi: 10.1109/RADECS.2016.8093169

34. R. Kaur, N. Surana and J. Mekie, "Guarded dual rail logic for soft error tolerant standard cell library," *2016 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Bremen, Germany, 2016, pp. 1-4.
doi: 10.1109/RADECS.2016.8093144

35. S. N. Ved, A. Gour, A. Arya and J. Mekie, "A holistic comparison of static VC allocation versus dynamic VC allocation based NoC routers," *2016 3rd International Conference on Emerging Electronics (ICEE)*, Mumbai, India, 2016, pp. 1-4.
doi: 10.1109/ICEmElec.2016.8074419

36. S. Teja, J. Mekie, J. -J. Cabibihan, N. V. Thakor and S. L. Kukreja, "Fault tolerant tactile sensor arrays for prosthesis," *2016 6th IEEE International Conference on Biomedical Robotics and Biomechatronics (BioRob)*, Singapore, 2016, pp. 31-34.
doi: 10.1109/BIOROB.2016.7523594

37. J. Mekie, "Effect of Dynamic Frequency Scaling on Interface Design for Rationally-Related Multi-clocked Systems," *2014 20th IEEE International Symposium on Asynchronous Circuits and Systems*, Potsdam, Germany, 2014, pp. 37-44.
doi: 10.1109/ASYNC.2014.13

38. J. Mekie and S. N. Ved, "Tutorial T7B: Network on Chips - The Journey Overview," *2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems*, Mumbai, India, 2014, pp. 18-18. doi: 10.1109/VLSID.2014.124

39. J. Mekie, S. Chakraborty, G. Venkataramani, P. S. Thiagarajan and D. K. Sharma, "Interface design for rationally clocked GALS systems," *12th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'06)*, Grenoble, France, 2006, pp. 12 pp.-171. doi: 10.1109/ASYNC.2006.19

40. J. Mekie, S. Chakraborty and D. K. Sharma, "Evaluation of pausible clocking for interfacing high speed IP cores in GALS framework," *17th International Conference on VLSI Design. Proceedings.*, Mumbai, India, 2004, pp. 559-564. doi: 10.1109/ICVD.2004.1260978

PROFESSIONAL SERVICES

- Reviewer for International Journals:
  - IEEE Design and Test, IEEE Sensors
  - IEEE Transactions on Circuits and Systems – II Express briefs
  - IEEE Transactions on Circuits and Systems – I: Regular papers
  - Microelectronics Reliability journal
  - Journal of IEEE Sensors
- Reviewer for National Journals:
  - Sadhana Academy proceedings in Engineering Science (SADH)
- Steering Committee member & PC member –
  - International Symposium on Asynchronous Circuits and Systems ASYNC 2015, ASYNC 2016, ASYNC 2017
- Techincal program committee member:
  - International Conference on VLSI Design and Embedded Systems – VLSI'15, VLSI'18, VLSI'19, VLSI'20
  - VLSI Design and Test – VDAT'17,
  - International Conference INDICON'13, INDICON'19
  - ISCAS'19, ISCAS'20, ISCAS'21, ISCAS'22
  - Education chair, IEEE VDAT 2015, Ahmedabad, India
  - Session chair, VLSID'18